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EXAMINER	
CHAUHAN, ULKA J	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/051,008	NAZANDA ET AL.	
	Examiner	Art Unit	
	Ulka J. Chauhan	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,18 and 20-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18 and 20-23* is/are allowed.

6)☒ Claim(s) *1-3,5-10,12-14 and 24-31* is/are rejected.

7)☒ Claim(s) *4 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 15-17, and 19 are cancelled; claims 1-14, 18, and 20-31 are pending.

Drawings

2. The drawings were received on 9/7/04. These drawings are acceptable.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 2, 8, 9, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,449,701 to Cho and U.S. Patent No. 6,272,600 to Talbot et al.

6. As per claims 1, 8, and 28, Cho teaches a computer system comprising processors 12A-12B, an L2 cache 14, and a memory controller 16 coupled to a memory 26, and a bus 24 for interconnecting the various components of system 10 [Fig. 1]. The memory controller 16 includes a request queue 40 ("***receive a plurality of data requests in a particular order***"), a

control circuit 50 and a data buffer 52 ("***buffer mechanism***"), coupled to receive information from bus 24 and are coupled to channel control circuits 42A-42B each including a memory queue 48 [c. 5 ll. 53-64 and Fig. 2]. Compare circuitry in request queue 40 sets an issued indication (Iss) to a state indicating that the transaction has been issued ("***simultaneously monitor a status of said plurality of data requests***") [c. 8 ll. 4-10 and Fig. 2]. Responsive to the data being ready, control circuit 50 arbitrates for the data bus 34 and transfers the data to the requesting agent ("***output responses to said plurality of data requests***") [c. 10 ll. 41-44]. Cho does not expressly teach outputting data "***in said particular order***". Talbot teaches a computer system in which a plurality of requests/memory addresses 303 are provided in an initial order and presented to a memory subsystem 216 according to a new ordering 311 to minimize waiting in the memory subsystem 216 caused by target addresses' not being available [c. 4 ll. 55-c. 5 ll. 4]. Data are read 324 from the memory subsystem 216 in the optimized order and are then reordered 313 into an order 312 corresponding to the initial request ordering, and returned ("***output responses to said plurality of data requests in said particular order***") [c. 5 ll. 5-15]. Talbot discloses that because data are returned 322 according to the initial request ordering, entities which request memory operations need not be aware of the order in which requested operations were actually executed by the memory subsystem 216 [c. 5 ll. 11-15]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the memory request reordering as taught by Talbot in combination with Cho's memory controller in order to optimize memory access execution without the memory access requestor being aware of the order in which requested operations were actually executed by the memory controller.

7. As per claims 2 and 9, Cho discloses that the control circuit 50 receives an acknowledge signal (Ack_I), a retry signal (Retry), a page inquire signal (Pg_i), a write signal (Wr), a read signal (Rd), and associated data buffer pointers (Ptr), and provides a hit signal (hit) [c. 6 ll. 23-31]. Data buffer 52 is coupled to receive the Ptr and Wr/Rd signals and to receive data from and provide data on the memory channel 44 [c. 6 ll. 37-39].

8. Claims 3, 5-7, 10, 12-14, 29, 30, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,449,701 to Cho and U.S. Patent No. 6,272,600 to Talbot et al and U.S. Patent No. 5,802,571 to Konigsburg et al.

9. As per claims 3, 6, 7, 10, 13, 14, 29, 30, and 31 Cho discloses that the memory controller 16 includes a control circuit 50 and a data buffer 52 [Fig. 2]. Cho does not expressly teach "***an age counter section***". Talbot discloses that an age of a request is determined by the timestamp associated with the request and that the address reordering unit schedules the oldest request [c. 6 ll. 56-60 and c. 7 ll. 19-22]. Konigsburg teaches a computer system in which a CPU 100 includes time-stamp units 156, that are preferably counters, for tagging requests with the age in which the requests were generated [c. 4 ll. 27-45], and an arbitration logic 154 for giving priority to the oldest request [c. 4 ll. 27-47]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the age counter as taught by Konigsburg in combination with Cho's memory controller and Talbot's request reordering in order to issue the oldest memory request and to maximize memory bandwidth while minimizing the amount of time that requests must wait to be serviced.

10. As per claims 5 and 12, Cho discloses that if a match is detected, control circuit 50 asserts a hit signal to channel control circuit 42, and the channel control circuit 42 keeps the page

open in response to the hit signal. In addition to asserting the hit signal, control circuit 50 sets the priority indication (Pr) to indicate high priority in each entry for which a match is detected [c. 9 ll. 36-47].

11. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,272,600 to Talbot et al.

12. As per claim 24, Talbot teaches a multiple-processor systems 201 and 202 [Figs. 2A, 2B] in which a plurality of requests/memory addresses 303 are provided in an initial order and presented to a memory subsystem 216 according to a new ordering 311 to minimize waiting in the memory subsystem 216 caused by target addresses' not being available [c. 4 ll. 55-c. 5 ll. 4], and returned data are reordered 313 into an order 312 corresponding to the initial request ordering [c. 5 ll. 5-15]. Talbot discloses that an age of a request is determined by the timestamp associated with the request and that the address reordering unit schedules the oldest request [c. 6 ll. 56-60 and c. 7 ll. 19-22]. Talbot discloses that because data are returned 322 according to the initial request ordering, entities which request memory operations need not be aware of the order in which requested operations were actually executed by the memory subsystem 216 [c. 5 ll. 11-15]. Talbot does not expressly teach "***graphics data requests***". It would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented Talbot's system within a graphics processing system for accessing graphics data in order to maximize memory bandwidth while minimizing the amount of time that graphics data requests must wait to be serviced.

13. Claims 25, 26, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,272,600 to Talbot et al and U.S. Patent No. 5,802,571 to Konigsburg et al.

14. As per claim 25, Talbot discloses that the request buffer 703 has a number of elements that can each store one request that is stored as a "type" 707, an "ID" 709, a "bank" 711, and a "valid" bit 713 that tells whether that element currently contains a request [c. 8 ll. 59-c. 9 ll. 5].

15. As per claims 26 and 27, Talbot discloses that the request buffer 703 is constructed as a shift register, with a younger end 705 and an opposite, older end 706, and that the age of entry of requests into the buffer 703 necessarily increases from the younger end 705 toward the older end 706 [c. 9 ll. 58-62]. Talbot does not expressly teach "***an age counter section***". Konigsburg teaches a computer system in which a CPU 100 includes time-stamp units 156, that are preferably counters, for tagging requests with the age in which the requests were generated [c. 4 ll. 27-45], and an arbitration logic 154 for giving priority to the oldest request [c. 4 ll. 27-47]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the age counter as taught by Konigsburg in combination with Talbot's invention 701 in order to easily determine and issue the oldest memory request and to maximize memory bandwidth while minimizing the amount of time that requests must wait to be serviced.

Allowable Subject Matter

16. Claims 18 and 20-23 are allowed.

17. Claims 4 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

18. The following is a statement of reasons for the indication of allowable subject matter: the cited prior art does not disclose or render obvious the combination of elements recited in the claims, as a whole. Specifically, the cited prior art fails to disclose or render obvious the following limitations: a multipurpose buffer mechanism comprising an age counter section, in turn comprising a plurality of shift registers as per claims 4, 11, 20.

Response to Arguments

19. With respect to claims 1 and 28, Applicant argues that Cho fails to teach at least simultaneously monitoring the status of the plurality of data requests. Applicant states that Cho discloses monitoring of the data buffer pointers returned by channel control circuit 42A and fails to disclose simultaneous monitoring of a status of a plurality of data requests. And further that the control circuit 50 is not monitoring the status of a data request in the buffer, rather, it is monitoring activities occurring outside of the buffer, namely in the memory. Cho discloses that each queue entry of request queue 40 stores an issued indication Iss [Figs. 2 and 3]. The issued indication, Iss, may be a bit, that when set indicates that the transaction has been issued, and when clear, indicates that the transaction has not been issued [c. 8 ll. 8-21]. Therefore, contrary to Applicant's assertion, Cho discloses monitoring the status of data requests; namely, through the Iss bit.

20. With respect to claim 24, Applicant argues that Talbot fails to disclose a "plurality of memory devices". Talbot, however discloses that a computing system in which the invention is embodied comprises memory subsystems including RAM subsystem 107, disk memory subsystem 109, tape memory subsystems, and networked server memory subsystems [c. 3 ll. 21-

36], and that a memory subsystem includes banks of memory [c. 7 ll. 28-43]; therefore, the memory subsystem includes plurality of memory devices.

21. Claims 8-10 and 12-14 were inadvertently left out of the rejection; as the scope of these claims is similar to the scope to claims 1-3 and 5-7, they were meant to be, and are rejected under the same rationale.

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ulka J. Chauhan whose telephone number is 571-272-7782. The examiner can normally be reached on Mon. through Fri., 9:30 a.m. to 4:00 p.m.
23. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 571-272-7778. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.
24. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ulka J. Chauhan
Primary Examiner
Art Unit 2676

ujc
March 5, 2005